EKLAVYA UNIVERSITY
ज्ञान प्राप्तये लक्ष्य संधानम्
Estd. by Madhya Pradesh Niji Vishvavidyalaya (Sthapna Evam Sanchalana) Adhyadesh, 2020

SCHOOL OF ENGINEERING

SYLLABUS

VLSI & EMBEDDED SYSTEMS

Class		M.TECH.	L	T	P	C
Semester/Year		I/I	3	-	-	3
Subject Name		RTL Simulation and Synthesis with PLDs				
Subject Code		MECVES20S101				
Paper	English					
	Hindi					
Max. Marks:		100				

Course Objective:

1. Familiarity of Finite State Machines, RTL design using reconfigurable logic, Design and develop IP **cores** Graphics and Xilinx.

Course Outcomes:
At the end of the course, students will demonstrate the ability to:
CO1: Understand familiarity of Finite State Machines, RTL design using reconfigurable logic.
CO2: Understand design and develop IP cores and Prototypes with performance guarantees
CO3: Understand use EDA tools like Cadence, Mentor Graphics and Xilinx.
CO4: Understand ASIC Design Flow.
CO5: Understand IP in various forms.

Unit	Syllabus	Periods
UNIT-I	Top down approach to design, Design of FSMs (Synchronous and asynchronous), Static timing analysis, Meta-stability, Clock issues, Need and design strategies for multi-clock domain designs.	8
UNIT-II	Design entry by SVerilog/VHDL/FSM, Verilog AMS.	9

UNIT-III	Programmable Logic Devices, Introduction to ASIC Design Flow, FPGA, SoC, Floor planning, Placement, Clock tree synthesis, Routing, Physical verification, Power analysis, ESD protection.	**11**
UNIT-IV	Design for performance, Low power VLSI & EMBEDDED SYSTEM design techniques. Design for testability.	**13**
UNIT-V	IP and Prototyping: IP in various forms: RTL Source code, Encrypted Source code, Soft IP, Netlist, Physical IP, Use of external hard IP during prototyping. Case studies and Speed issues.	**14**
	Text Book(s): 1. Bob Zeidman, "Designing with FPGAs & CPLDs", CMPBooks. 2. Charles Roth, Jr. and Lizy K John, "Digital System Design using VHDL",Cengage.	
	References Book: 1. Richard S. Sandige, "Modern Digital Design", MGH, InternationalEditions. 2. Donald D Givone, "Digital principles and Design",TMH 3. Charles Roth, Jr. and Lizy K John, "Digital System Design using VHDL",Cengage. 4. Samir Palnitkar, "Verilog HDL, a guide to digital design and synthesis", PrenticeHall. 5. Doug Amos, Austin Lesea, Rene Richter, "FPGA based prototyping methodology manual",Xilinx 6. Bob Zeidman, "Designing with FPGAs & CPLDs", CMPBooks.	

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Class		**M.TECH.**	**L**	**T**	**P**	**C**
Semester/Year		**I/I**	**3**	**-**	**-**	**5**
Subject Name		**Microcontrollers and Programmable Digital Signal Processors**				
Subject Code		**MECVES20S102**				
Paper	**English**					
	Hindi					
Max. Marks:		**100**				

Course Objective:

1. To understand CISC and RISC Architectures To Learn ARM processor , DSP Processors.

Course Outcomes:

At the end of this course, students will be able to

CO1: Compare and select ARM processor core based SoC with several features/peripheral based on requirements of embedded applications.

CO2: Identify and characterize architecture of Programmable DSP Processors

CO3: Develop small applications by utilizing the ARM processor core and DSP processor based platform.

CO4: Understand Harvard architecture.

CO5: Understand of different architecture study.

Unit	Syllabus	Periods
UNIT-I	ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive	**8**

	Transfers. Pipeline, Bus Interfaces	
UNIT-II	Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behaviour, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.	**9**
UNIT-III	LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT.	**11**
UNIT-IV	Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family.	**13**
UNIT-V	VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations. Code Composer Studio for application development for digital signal processing, On chip peripherals , Processor benchmarking.	**14**
	Text Book(s): **1.** Daniel Tabak, "Advanced Microprocessors", McGraw Hill Inc., 1995 **2.** David E Simon "An Embedded Software Primer", Pearson Education, 2007	
	References Book: 1. Joseph Yiu, "The definitive guide to ARM Cortex-M3", Elsevier, 2nd Edition 2. Venkatramani B. and Bhaskar M. "Digital Signal Processors: Architecture, Programming and Applications" , TMH , 2nd Edition 3. Sloss Andrew N, Symes Dominic, Wright Chris, "ARM System Developer's Guide: Designing and Optimizing", Morgan KaufmanPublication 4. Steve furber, "ARM System-on-Chip Architecture", PearsonEducation 5. Frank Vahid and Tony Givargis, "Embedded System Design",Wiley.	

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Class		**M.TECH.**	**L**	**T**	**P**	**C**
Semester/Year		**I/I**	**3**	**-**	**-**	**3**
Subject Name		**Digital Signal and Image Processing**				
Subject Code		**MECVES20S103**				
Paper	**English**					
	Hindi					
Max. Marks:		**100**				

Course Objective:

1. Digital Signal Processor basics Third generation DSP Architecture and programming skills.
2. Advanced DSP architectures and some applications.

Course Outcomes:

At the end of this course, students will be able to:

CO1: Analyze discrete-time signals and systems in various domains

CO2: Design and implement filters using fixed point arithmetic targeted for embedded platforms

CO3: Compare algorithmic and computational complexities in processing and coding digital images.

CO4: Design sDSP based System Developer.

CO5: Understand Color Image processing.

Unit	Syllabus	Periods
UNIT-I	Review of Discrete Time signals and systems, Characterization in time and Z and Fourier – domain, Fast Fourier Transform algorithms – In-place computations, Butterfly computations, bit reversal's.	**8**

UNIT-II	Digital Filter design: FIR - Windowing and Frequency Sampling, IIR – Impulse invariance, bilinear Transformation.	**9**
UNIT-III	Fixed point implementation of filters – challenges and techniques.	**11**
UNIT-IV	Digital Image Acquisition, Enhancement, Restoration. Digital Image Coding and Compression – JPEG and JPEG 2000.	**13**
UNIT-V	Colour Image processing – Handling multiple planes, computational challenges. VLSI & EMBEDDED SYSTEM architectures for implementation of Image Processing algorithms, Pipelining.	**14**
	Text Book(s): 1. User guides Texas Instrumentation, Analog Devices, Motorola. 2. Schalkoff R.J., "Digital Image Processing & Computer Vision", John Wiley & Sons, 1992.	
	References Book: 1. J.G. Proakis, Manolakis "Digital Signal Processing", Pearson, 4th Edition 2. Gonzalez and Woods, "Digital Image Processing", PHI, 3rd Edition 3. S. K. Mitra. "Digital Signal Processing – A Computer based Approach", TMH, 3rd Edition, 2006 4. A. K. Jain, "Fundamentals of Digital Image Processing", PrenticeHall 5. KeshabParhi, "VLSI & EMBEDDED SYSTEM Digital Signal Processing Systems – Design and Implementation", WileyIndia	

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VLSI & EMBEDDED SYSTEM

Class		**M.TECH.**	**L**	**T**	**P**	**C**
Semester/Year		**I/I**	**3**	**-**	**-**	**3**
Subject Name		**Programming Languages for Embedded Software**				
Subject Code		**MECVES20S104**				
Paper	**English**					
	Hindi					
Max. Marks:		**100**				

Course Objective:

1. Learn design challenges and design methodologies Study general and single purpose processor.. U

Course Outcomes:

At the end of this course, students will be able to

CO1: Write an embedded C application of moderate complexity.
CO2: Develop and analyze algorithms in C++.
CO3: Differentiate interpreted languages from compiled languages.
CO4: Overloading and Inheritance.
CO5: Understand Scripting Languages.

Unit	Syllabus	Periods
UNIT-I	Embedded 'C' Programming, Bitwise operations, Dynamic memory allocation, OS services, Linked stack and queue, Sparse matrices, Binary tree, Interrupt handling in C, Code optimization issues. Writing LCD drives, LED drivers, Drivers for serial port communication. Embedded Software	**8**

	Development Cycle and Methods (Waterfall, Agile).	
UNIT-II	Object Oriented Programming, Introduction to procedural, modular, object-oriented and generic programming techniques, Limitations of procedural programming, objects, classes, data members, methods, data encapsulation, data abstraction and information hiding, inheritance, polymorphism.	**9**
UNIT-III	CPP Programming: 'cin', 'cout', formatting and I/O manipulators, new and delete operators, Defining a class, data members and methods, 'this' pointer, constructors, destructors, friend function, dynamic memory allocation.	**11**
UNIT-IV	Overloading and Inheritance: Need of operator overloading, overloading the assignment, overloading using friends, type conversions, single inheritance, base and derived classes, friend classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, polymorphism, virtual functions.	**13**
UNIT-V	Templates: Function template and class template, member function templates and template arguments, Exception Handling: syntax for exception handling code: try-catch-throw, Multi Exceptions. Scripting Languages Overview of Scripting Languages – PERL, CGI, VB Script, Java Script. PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables, Inter process Communication Threads, Compilation & Line Interfacing.	**14**
	Text Book(s): 1. Frank Vahid and Tony Gwargie, "Embedded System Design", John Wiley & sons, 2002. 2. Steve Heath, "Embedded System Design", Elsevier, Second Edition, 2004.	
	References Book: 1. Michael J. Pont , "Embedded C", Pearson Education, 2nd Edition,2008. 2. Randal L. Schwartz, "Learning Perl", O'Reilly Publications, 6th Edition2011. 3. A. Michael Berman, "Data structures via C++", Oxford University Press,2002. 4. Robert Sedgewick, "Algorithms in C++", Addison Wesley Publishing Company,1999.	

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Class		M.TECH.	L	T	P	C
Semester/Year		I/I	3	-	-	3
Subject Name		VLSI & EMBEDDED SYSTEM SIGNAL PROCESSING				
Subject Code		MECVES20S105				
Paper	English					
	Hindi					
Max. Marks:		100				

Course Objective:

1. To introduce techniques for altering the existing DSP structures to suit VLSI implementations.
2. To introduce efficient design of DSP architectures suitable for VLSI & EMBEDDED SYSTEM.

Course Outcomes:

At the end of this course, students will be able to

CO1: Acquired knowledge about DSP algorithms, its DFG representation, pipelining and parallel processing approaches.

CO2: Ability to acquire knowledge about retiming techniques, folding and register minimization path problems.

CO3: Ability to have knowledge about algorithmic strength reduction techniques and parallel processing of FIR and IIR digital filters.

CO4: Acquired knowledge about finite word-length effects and round off noise computation in DSP systems.

CO5: Ability to modify the existing or new DSP architectures suitable for VLSI & EMBEDDED SYSTEM.

Unit	Syllabus	Periods
UNIT-I	Introduction to DSP systems, Pipelined and parallel processing.	**8**
UNIT-II	Iteration Bound, Retiming, unfolding, algorithmic strength reduction in filters and Transforms.	**9**
UNIT-III	Systolic architecture design, fast convolution, pipelined and parallel recursive and adaptive filters, Scaling and round off noise.	**11**
UNIT-IV	Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic.	**13**
UNIT-V	Numerical strength reduction, synchronous, wave and asynchronous pipe lines, low power design. Programmable digit signal processors.	**14**
	Text Book(s): **1.** Keshab K. Parhi, " VLSI& EMBEDDED SYSTEM Digital Signal Processing Systems, Design and implementation ", Wiley, Interscience, 2007. 2. U. Meyer – Baese, " Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition, 2004.	
	References Book: 1. KeshabK. Parthi[A1], VLSI & EMBEDDED SYSTEM Digital signal processing systems, design and implementation[A2], Wiley, Inter Science,1999. 2. Mohammad Isamail and Terri Fiez, AnalogVLSI & EMBEDDED SYSTEM signal and information processing, McGraw Hill,1994 3. S.Y. Kung, H.J. White House, T. Kailath, VLSI & EMBEDDED SYSTEM and Modern Signal Processing, Prentice Hall,1985.	

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Class		**M.TECH.**	**L**	**T**	**P**	**C**
Semester/Year		**I/I**	**3**	**-**	**-**	**3**
Subject Name		**Parallel Processing**				
Subject Code		**MECVES20S106**				
Paper	**English**					
	Hindi					
Max. Marks:		**100**				

Course Objective:

1. Overview of Parallel Processing and Pipelining, pipelining techniques, VLIW processors, Operating systems for multiprocessors systems.

Course Outcomes:

At the end of this course, students will be able to:
CO1: Identify limitations of different architectures of computer
CO2: Analyse quantitatively the performance parameters for different architectures
CO3: Investigate issues related to compilers and instruction set based on type of architectures.
CO4: Understand Multithreading.
CO5: Perform parallel Programming Techniques.

Unit	Syllabus	Periods
UNIT-I	Overview of Parallel Processing and Pipelining, Performance analysis, Scalability.	**8**
UNIT-II	Principles and implementation of Pipelining, Classification of pipelining processors, Advanced pipelining techniques, Software pipelining.	**9**

UNIT-III	VLIW processors Case study: Superscalar Architecture- Pentium, Intel Itanium Processor, Ultra SPARC, MIPS on FPGA, Vector and Array Processor, FFT Multiprocessor Architecture.	**11**
UNIT-IV	Multithreaded Architecture, Multithreaded processors, Latency hiding techniques, Principles of multi threading, Issues and solutions.	**13**
UNIT-V	Parallel Programming Techniques: Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming, Data Parallel Programming, Parallel Software Issues. Operating systems for multiprocessors systems Customizing applications on parallel processing platforms.	**14**
	Text Book(s): 1. Kai Hwang, ZhiweiXu, "Scalable Parallel Computing",MGH. 2. V. Rajaraman, L. Sivaram Murthy, "Parallel Computers",PHI.	
	References Book: 1. KaiHwang,Faye A. Briggs, "Computer Architecture and Parallel Processing", MGH InternationalEdition 2. Kai Hwang, "Advanced Computer Architecture",TMH 3. V. Rajaraman, L. Sivaram Murthy, "Parallel Computers",PHI. 4. William Stallings, "Computer Organization and Architecture, Designing for performance" Prentice Hall, Sixthedition 5. Kai Hwang, ZhiweiXu, "Scalable Parallel Computing",MGH 6. David Harris and Sarah Harris, "Digital Design and Computer Architecture", Morgan Kaufmann.	

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Class		**M.TECH.**	**L**	**T**	**P**	**C**
Semester/Year		**I/I**	**3**	**-**	**-**	**3**
Subject Name		**System Design with Embedded Linux**				
Subject Code		**MECVES20S107**				
Paper	**English**					
	Hindi					
Max. Marks:		**100**				

Course Objective:

1. To expose the students to the fundamentals of embedded system design. To enable the students to understand and use embedded computing platform. To introduce networking principles in embedded devices.
2. To introduce RTOS in embedded devices.

Course Outcomes:

At the end of this course, students will be able to:
CO1: Understand the familiarity of the embedded Linux development model.
CO2: Write, debug, and profile applications and drivers in embedded Linux.
CO3: Understand and create Linux BSP for a hardware platform.
CO4: Develop Porting Applications.
CO5: Perform building and Debugging.

Unit	Syllabus	Periods
UNIT-I	Embedded Linux Vs Desktop Linux, Embedded Linux Distributions.	**8**
UNIT-II	Embedded Linux Architecture, Kernel Architecture – HAL, Memory manager, Scheduler, File System, I/O and Networking subsystem, IPC, space, Start-up sequence.	**9**

UNIT-III	Board Support Package Embedded Storage: MTD, Architecture, Drivers, Embedded File System Embedded Drivers: Serial, Ethernet, I^2C, USB, Timer, Kernel Modules.	**11**
UNIT-IV	Porting Applications. Real-Time Linux: Linux and Real time, Programming, Hard Real-time Linux.	**13**
UNIT-V	Building and Debugging: Kernel, Root file system. Embedded Graphics. Case study of uClinux	**14**
	Text Book(s): 1. Jane.W.S. Liu, "Real-Time systems", Pearson Education Asia. 2. C. M. Krishna and K. G. Shin, "Real-Time Systems" , McGraw-Hill, 1997.	
	References Book: 1. KarimYaghmour, "Building Embededd Linux Systems", O'Reilly &Associates. 2. P Raghvan, Amol Lad, SriramNeelakandan, "Embedded Linux System Design and Development", Auerbach Publications. 3. Christopher Hallinan, "Embedded Linux Primer: A Practical Real World Approach", Prentice Hall, 2nd Edition,2010. 4. Derek Molloy, "Exploring BeagleBone: Tools and Techniques for Building with Embedded Linux", Wiley, 1stEdition,2014.	

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VLSI & EMBEDDED SYSTEM

Class		M.TECH.	L	T	P	C
Semester/Year		I/I	3	-	-	3
Subject Name		CAD of Digital System				
Subject Code		MECVES20S108				
Paper	English					
	Hindi					
Max. Marks:		100				

Course Objective:
1.Fundamentals of CAD tools for modeling, VLSI & EMBEDDED SYSTEM systems.
2.To implement sMCMS-VHDL-Verilog.

Course Outcomes:
CO1: Fundamentals of CAD tools for modelling, design, test and verification of VLSI & EMBEDDED SYSTEM systems.
CO2: Study of various phases of CAD, including simulation, physical design, test and verification.
CO3: Demonstrate knowledge of computational algorithms and tools for CAD.
CO4: Simulation – logic synthesis.
CO5: Implementation of simple circuits using VHDL.

Unit	Syllabus	Periods
UNIT-I	Introduction to VLSI & EMBEDDED SYSTEM Methodologies – Design and Fabrication of VLSI & EMBEDDED SYSTEM Devices, Fabrication Process and its impact on Design.	8
UNIT-II	VLSI & EMBEDDED SYSTEM design automation tools – Data structures and basic algorithms, graph theory and mutational complexity, tractable and intractable problems.	9

UNIT-III	General purpose methods for combinational optimization – partitioning, floor planning and pin assignment, placement, routing.	**11**
UNIT-IV	Simulation – logic synthesis, verification, high level Synthesis.	**13**
UNIT-V	MCMS-VHDL-Verilog-implementation of simple circuits using VHDL.	**14**
	Text Book(s): 1. Charles H.RothJr "Fundamentals of Logic Design" Thomson Learning 2004. 2. ParagK.Lala "Digital system Design using PLD" B S Publications,2003	
	References Book. 1. N.A. Sherwani, "Algorithms for VLSI & EMBEDDED SYSTEM Physical DesignAutomation". 2. S.H. Gerez, "Algorithms for VLSI & EMBEDDED SYSTEM DesignAutomation. 3. S. Palnitkar , Verilog HDL – A Guide to Digital Design and Synthesis, Pearson , 2003.	

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VLSI & EMBEDDED SYSTEM

Class		**M.TECH.**	**L**	**T**	**P**	**C**
Semester/Year		**I/I**	**2**	**-**	**-**	**-**
Subject Name		**English for Research Paper Writing**				
Subject Code		**MECVES20S109**				
Paper	**English**					
	Hindi					
Max. Marks:		**-**				

Course Objective:

1. Understand that how to improve your writing skills and level of readability Learn about what to write in each section. Understand the skills needed when writing a Title Ensure the good quality of paper at very first-time submission

Course outcomes:

At the end of this course, students will be able to:
CO1: Understand that how to improve your writing skills and level of readability.
CO2: Learn about what to write in each section.
CO3: Understand the skills needed when writing a Title Ensure the good quality of paper at very first-time submission.
CO4: Understand Key skills.
CO5: Understand writing the Discussion.

Unit	Syllabus	Periods
UNIT-I	Planning and Preparation, Word Order, breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness.	**8**

UNIT-II	Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts.	**9**
UNIT-III	Introduction. Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.	**11**
UNIT-IV	Key skills needed when writing a Title, key skills needed when writing an Abstract, key skills needed when writing an Introduction, skills needed when writing a Review of the Literature, skills needed when writing the Methods, skills needed when writing the Results.	**13**
UNIT-V	Skills needed when writing the Discussion, skills are needed when writing the Conclusions, useful phrases, how to ensure paper is as good as it could possibly be the first- time submission..	**14**
	Text Book(s): 1. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London,2011. 2. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman'sbook.	
	References Book: 1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books). 2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press. 3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book. 4. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London,2011.	

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Class		**M.TECH.**	**L**	**T**	**P**	**C**
Semester/Year		**I/I**	**-**	**-**	**4**	**2**
Subject Name		**RTL Simulation and Synthesis with PLDs Lab**				
Subject Code		**MECVES20S110**				
Paper	**English**					
	Hindi					
Max. Marks:		**50**				

List of Experiments:

1) Verilog implementation of 8:1 Mux/Demux, Full Adder, 8-bit Magnitude comparator, Encoder/decoder, Priority encoder, D-FF, 4-bit Shift registers (SISO, SIPO, PISO, bidirectional), 3-bit Synchronous Counters, Binary to Gray converter, Paritygenerator.
2) Sequence generator/detectors, Synchronous FSM – Mealy and Mooremachines.
3) Vending machines - Traffic Light controller, ATM, elevatorcontrol.
4) PCI Bus & arbiter and downloading on FPGA.
5) UART/ USART implementation inVerilog.
6) Realization of single port SRAM inVerilog.

Verilog implementation of Arithmetic circuits like serial adder/ subtractor, parallel adder/subtractor, serial/parallel multiplier. Discrete Fourier transform/Fast Fourier Transform algorithm inVerilog.

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Class		**M.TECH.**	**L**	**T**	**P**	**C**
Semester/Year		**I/I**	**2**	**-**	**-**	**2**
Subject Name		**Research Methodology and IPR**				
Subject Code		**MMAT20S111**				
Paper	**English**					
	Hindi					
Max. Marks:		**100**				

Course Objective:

1. Understand research problem formulation. Analyze research related in Formation.
2. Follow research ethics, IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.

Course Outcomes:

At the end of this course, students will be able to:

CO1: Identify limitations of different architectures of computer

CO2: Analyse quantitatively the performance parameters for different architectures

CO3: Investigate issues related to compilers and instruction set based on type of architectures.

CO4: Understand Multithreading.

CO5: Understand parallel Programming Techniques.

Unit	Syllabus	Periods
UNIT-I	Overview of Parallel Processing and Pipelining, Performance analysis, Scalability.	**8**
UNIT-II	Principles and implementation of Pipelining, Classification of pipelining processors, Advanced pipelining techniques, Software pipelining.	**9**

UNIT-III	VLIW processors Case study: Superscalar Architecture- Pentium, Intel Itanium Processor, Ultra SPARC, MIPS on FPGA, Vector and Array Processor, FFT Multiprocessor Architecture.	**11**
UNIT-IV	Multithreaded Architecture, Multithreaded processors, Latency hiding techniques, Principles of multi threading, Issues and solutions.	**13**
UNIT-V	Parallel Programming Techniques: Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming, Data Parallel Programming, Parallel Software Issues. Operating systems for multiprocessors systems Customizing applications on parallel processing platforms.	**14**
	Text Book(s): 1. Kai Hwang, ZhiweiXu, "Scalable Parallel Computing",MGH. 2. V. Rajaraman, L. Sivaram Murthy, "Parallel Computers",PHI.	
	References Book: 1. KaiHwang,Faye A. Briggs, "Computer Architecture and Parallel Processing", MGH InternationalEdition 2. Kai Hwang, "Advanced Computer Architecture",TMH 3. V. Rajaraman, L. Sivaram Murthy, "Parallel Computers",PHI. 4. William Stallings, "Computer Organization and Architecture, Designing for performance" Prentice Hall, Sixthedition 5. Kai Hwang, ZhiweiXu, "Scalable Parallel Computing",MGH 6. David Harris and Sarah Harris, "Digital Design and Computer Architecture", Morgan Kaufmann.	

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SCHOOL OF ENGINEERING

SYLLABUS

VLSI & EMBEDDED SYSTEMS

Class		**M.TECH.**	**L**	**T**	**P**	**C**
Semester/Year		**I/I**	**-**	**-**	**4**	**2**
Subject Name		**Microcontrollers and Programmable Digital Signal Processors Lab**				
Subject Code		**MECVES20S112**				
Paper	**English**					
	Hindi					
Max. Marks:		**50**				

List of Experiments:

Part A) Experiments to be carried out on Cortex-M3 development boards and using GNU tool chain

1. Blink an LED with software delay, delay generated using the Sys Tick timer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hard ware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.
5. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
6. Temperature indication on an RGBLED.
7. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
8. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
9. System reset using watchdog timer in case something goes wrong.
10. Sample sound using a microphone and display sound levels onLEDs.

Part B) Experiments to be carried out on DSP C6713 evaluation kits and using Code Composer Studio (CCS)

1. To develop an assembly code and C code to compute Euclidian distance between any two points
2. To develop assembly code and study the impact of parallel, serial and mixedexecution
3. To develop assembly and C code for implementation of convolution operation
4. To design and implement filters in C to enhance the features of given input sequence/signal.

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VLSI & EMBEDDED SYSTEM

Class		**M.TECH.**	**L**	**T**	**P**	**C**
Semester/Year		**II/I**	**3**	**-**	**-**	**3**
Subject Name		**Analog and Digital CMOS VLSI Design**				
Subject Code		**MECVES20S201**				
Paper	**English**					
	Hindi					
Max. Marks:		**100**				

Course Objective:

1. MOS structure, CMOS inverter, Sequential logic: Static latches and registers, MOS structure, Passive and active current mirrors.

Course Outcomes:

At the end of this course, students will be able to:

CO1: Analyze, design, optimize and simulate analog and digital circuits using CMOS constrained by the design metrics.

CO2: Connect the individual gates to form the building blocks of a system.

CO3: Use EDA tools like Cadence, Mentor Graphics and other open source software tools like Ngspice.

CO4: Understand Single Stage Amplifier.

CO5: Understand different types of mirrors.

Unit	Syllabus	Periods
UNIT-I	Review: Basic MOS structure and its static behavior, Quality metrics of a digital design: Cost, Functionality, Robustness, Power, and Delay, Stick diagram and Layout, Wire delay models. Inverter: Static CMOS inverter,	**8**

	Switching threshold and noise margin concepts and their evaluation, Dynamic behaviour, Power consumption.	
UNIT-II	Physical design flow: Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation-static and dynamic, ESD protection-human body model, Machine model. Combinational logic: Static CMOS design, Logic effort, Rationed logic, Pass transistor logic, Dynamic logic, Speed and power dissipation in dynamic logic, Cascading dynamic gates, CMOS transmission gate logic.	**9**
UNIT-III	Sequential logic: Static latches and registers, Bi-stability principle, MUX based latches, Static SR flip-flops, Master-slave edge-triggered register, Dynamic latches and registers, Concept of pipelining, Pulse registers, Non-bistable sequential circuit. Advanced technologies: Giga-scale dilemma, Short channel effects, High–k, Metal Gate. Technology, Fin FET, TFET etc.	**11**
UNIT-IV	Single Stage Amplifier: CS stage with resistance load, Divide connected load, Current source load, Triode load, CS stage with source degeneration, Source follower, Common-gate stage, Cascade stage, Choice of device models. Differential Amplifiers: Basic difference pair, Common mode response, Differential pair with MOS loads, Gilbert cell.	**13**
UNIT-V	Passive and active current mirrors: Basic current mirrors, Cascade mirrors, Active current mirrors. Frequency response of CS stage: Source follower, Common gate stage, Cascade stage and difference pair, Noise. Operational amplifiers: One stage OPAMP, Two stage OPAMP, Gain boosting, Common mode feedback, Slew rate, PSRR, Compensation of 2 stage OPAMP, Other compensation techniques.	**14**
	Text Book(s): 1. Baker, Li, Boyce, "CMOS Circuit Design, Layout, and Simulation", Wiley, 2nd Edition. 2. Kang, S. and Leblebici, Y., "CMOS Digital Integrated Circuits, Analysis and Design", TMH, 3rd Edition.	
	References Book: 1. J P Rabaey, A P Chandrakasan, B Nikolic, "Digital Integrated circuits: A design perspective", Prentice Hall electronics and VLSI & EMBEDDED SYSTEM series, 2nd Edition. 2. Baker, Li, Boyce, "CMOS Circuit Design, Layout, and Simulation", Wiley, 2nd Edition. 3. Behzad Razavi , "Design of Analog CMOS Integrated Circuits", TMH,2007. 4. Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford, 3rd Edition. **5.** R J Baker, "CMOS circuit Design, Layout and Simulation", IEEE .	

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VLSI & EMBEDDED SYSTEM

Class		M.TECH.	L	T	P	C
Semester/Year		II/I	3	-	-	3
Subject Name		VLSI & EMBEDDED SYSTEM Design Verification and Testing				
Subject Code		MECVES20S202				
Paper	English					
	Hindi					
Max. Marks:		100				

Course Object:

1. Identify sources of power in an IC. Identify the power reduction techniques based on technology independent and technology dependent Power dissipation mechanism in various MOS logic style. Identify suitable techniques to reduce the power dissipation. Design memory circuits with low power dissipation.

Course Outcomes:

At the end of this course, students will be able to:

CO1: Familiarity of Front end design and verification techniques and create reusable test environments.

CO2: Verify increasingly complex designs more efficiently and effectively.

CO3: Use EDA tools like Cadence, Mentor Graphics.

CO4: Understand system Verilog Assertions: Basic OOP.

CO5: Understand randomization: Introduction, **:**Random number functions.

Unit	Syllabus	Periods
UNIT-I	Verification guidelines: Verification Process, Basic Test bench functionality, directed testing, Methodology basics, Constrained-Random stimulus, Functional coverage, Test bench components, Layered test bench, Building	**8**

	layered test bench, Simulation environment phases, Maximum code reuse, Test bench performance.	
UNIT-II	Data types: Built-in data types, Fixed-size arrays, Dynamic arrays, Queues, Associative arrays, Linked lists, Array methods, Choosing a storage type, Creating new types with typedef , Creating user-defined structures, Type conversion, Enumerated types, Constants strings, Expression width.	**9**
UNIT-III	Procedural statements and routines: Procedural statements, tasks, functions and void functions, Routine arguments, Returning from a routine, Local data storage, Time values Connecting the testbench and design: Separating the testbench and design, Interface constructs, Stimulus timing, Interface driving and sampling, Connecting it all together, Top-level scope Program – Module interactions.	**11**
UNIT-IV	System Verilog Assertions: Basic OOP: Introduction, think of nouns, Not verbs, your first class, where to define a class, OOP terminology, Creating new objects, Object de-allocation, Using objects, Static variables vs. Global variables, Class methods, Defining methods outside of the class, Scoping rules, Using one class inside another, Understanding dynamic objects, Copying objects, Public vs. Local, Straying off course building a test bench.	**13**
UNIT-V	Randomization: Introduction, What to randomize, Randomization in System Verilog, Constraint details solution probabilities, Controlling multiple constraint blocks, Valid constraints, In-line constraints, The pre_randomize and post_randomize functions. Random number functions, Constraints tips and techniques, Common randomization problems, Iterative and array constraints, Atomic stimulus generation vs. Scenario generation, Random control, Random number generators, Random device configuration.	**14**
	Text Book(s): **1.** J.B.Kulo and J.H Lou, “Low voltage CMOS VLSI & EMBEDDED SYSTEM Circuits”, Wiley 1999 2. A.P.Chandrasekaran and R.W.Broadersen, “Low power digital CMOS design”, Kluwer,1995.	
	References Book: 1. Chris Spears, “ System Verilog for Verification”, Springer, 2nd Edition 2. M. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI & EMBEDDED SYSTEM Circuits", Kluwer AcademicPublishers 3. IEEE 1800-2009 standard (IEEE Standard for SystemVerilog—Unified Hardware Design,Specification, and Verification Language). 4. System Verilog website –www.systemverilog.org	

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SYLLABUS

VLSI & EMBEDDED SYSTEM

Class		M.TECH.	L	T	P	C
Semester/Year		II/I	3	-	-	3
Subject Name		Memory Technologies				
Subject Code		MECVES20S203				
Paper	English					
	Hindi					
Max. Marks:		100				

Course Objective:

1. Comprehensive understanding of Static Random Access Memory (SRAMs), Dynamic Random Access Memory (DRAM) and Nonvolatile Memory Architectures and their feature comparison.

Course Outcomes:

At the end of the course, students will be able to:

CO1: Select architecture and design semiconductor memory circuits and subsystems.
CO2: Identify various fault models, modes and mechanisms in semiconductor memories and their testing procedures.
CO3: Know-how of the state-of-the-art memory chip design.
CO4: Understand Semiconductor Memory.
CO5: Implement Advanced Memory Technologies and High-density Memory Packing Technologies.

Unit	Syllabus	Periods
UNIT-I	Random Access Memory Technologies: Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.	8

UNIT-II	DRAMs, MOS DRAM Cell, Bi CMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs. SRAM and DRAM Memory controllers.	**9**
UNIT-III	Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.	**11**
UNIT-IV	Semiconductor Memory Reliability and Radiation Effects: General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing.	**13**
UNIT-V	Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices. Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards,High Density Memory Packaging.	**14**
	Text Book(s): **1.** KiyooItoh, "VLSI & EMBEDDED SYSTEM memory chip design", Springer International Edition. **2.** Ashok K Sharma," Semiconductor Memories: Technology, Testing and Reliability ,PHI.	
	References Book: 1. Ashok K Sharma, "Advanced Semiconductor Memories: Architectures, Designs and Applications", WileyInterscience 2. KiyooItoh, "VLSI & EMBEDDED SYSTEM memory chip design", Springer InternationalEdition 3. Ashok K Sharma," Semiconductor Memories: Technology, Testing and Reliability ,PHI	

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VLSI & EMBEDDED SYSTEM

Class		M.TECH.	L	T	P	C
Semester/Year		II/I	3	-	-	3
Subject Name		SoC Design				
Subject Code		MECVES20S204				
Paper	English					
	Hindi					
Max. Marks:		100				

Course Objective:

1. ASIC, NISC, Simulation, Low power SoC design / Digital system, Synthesis.

Course Outcomes:

At the end of the course, students will be able to:

CO1: Identify and formulate a given problem in the framework of SoC based design approaches.
CO2: Design SoC based system for engineering applications.
CO3: Realize impact of SoC on electronic design philosophy and Macro-electronics thereby incline towards entrepreneurship &skill development.
CO4: Understand Design synergy.
CO5: Understand Role and Concept of graph theory.

Unit	Syllabus	Periods
UNIT-I	Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts.	**8**
UNIT-II	NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction- set Processors (ASIP), No-Instruction-	**9**

	Set-computer (NISC)- design flow, modelling NISC architectures and systems, use of Generic Net list Representation - A formal language for specification, compilation and synthesis of embedded processors.	
UNIT-III	Different simulation modes, behavioural, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modelling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.	**11**
UNIT-IV	Design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.	**13**
UNIT-V	Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysis Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs. Case study for overview of cellular phone design with emphasis on area optimization, speed improvement and power minimization.	**14**
	Text Book(s): 1. B. Al Hashimi, “System on chip-Next generation electronics”, The IET,2006. 2. P Mishra and N Dutt, “Processor Description Languages”, Morgan Kaufmann,2008	
	References Book: 1. Hubert Kaeslin, “Digital Integrated Circuit Design: From VLSI & EMBEDDED SYSTEM Architectures to CMOS Fabrication”, Cambridge University Press,2008. 2. B. Al Hashimi, “System on chip-Next generation electronics”, The IET,2006 3. RochitRajsuman, “System-on- a-chip: Design and test”, Advantest America R & D Center, 2000 4. P Mishra and N Dutt, “Processor Description Languages”, Morgan Kaufmann,2008 5. Michael J. Flynn and Wayne Luk, “Computer System Design: System-on-Chip”. Wiley, 2011	

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SYLLABUS

VLSI & EMBEDDED SYSTEM

Class		M.TECH.	L	T	P	C
Semester/Year		II/I	3	-	-	3
Subject Name		Low Power VLSI & EMBEDDED SYSTEM Design				
Subject Code		MECVES20S205				
Paper	English					
	Hindi					
Max. Marks:		100				

Course Objective:

1. Technology & Circuit Design Levels, Low Power Circuit Techniques, Logic Synthesis for Low Power estimation techniques.

Course Outcomes:

At the end of the course, students will be able to:

CO1: Identify the sources of power dissipation in digital IC systems & understand the impact of power on system performance and reliability.

CO2: Characterize and model power consumption & understand the basic analysis methods.

CO3: Understand leakage sources and reduction techniques.

CO4: Implement Logic Synthesis for Low Power estimation techniques.

CO5: Understand Low Power Memory Design.

Unit	Syllabus	Periods
UNIT-I	Technology & Circuit Design Levels: Sources of power dissipation in digital ICs, degree off redeem, recurring themes in low-power, emerging low power approaches, dynamic dissipation in CMOS, effects of Vdd&Vt on speed, constraints on Vt reduction, transistor sizing & optimal gate	8

	oxide thickness, impact of technology scaling, technology innovations.	
UNIT-II	Low Power Circuit Techniques: Power consumption in circuits, flip flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches.	**9**
UNIT-III	Low Power Clock Distribution: Power dissipation in clock distribution, single driver versus distributed buffers, buffers & device sizing under process variations, zero skew Vs. tolerableskew, chip & package co-design of clock network.	**11**
UNIT-IV	Logic Synthesis for Low Power estimation techniques: Power minimization techniques, low power arithmetic components- circuit design styles, adders, multipliers.	**13**
UNIT-V	Low Power Memory Design: Sources & reduction of power dissipation in memory subsystem, sources of power dissipation in DRAM & SRAM, low power DRAM circuits, low power SRAM circuits. Low Power Microprocessor Design System: power management support, architectural trade offs for power, choosing the supply voltage, low-power clocking, implementation problem for low power, comparison of microprocessors for power & performance.	**14**
	Text Book(s): 1. J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI & EMBEDDED SYSTEM Circuits", Wiley,1999. 2. A. P. Chandrasekaran and R.W.Broadersen,"Low power digitalCMOS design", Kluwer,1995	
	References Book: 1. P. Rashinkar, Paterson and L. Singh, "Low Power Design Methodologies", Kluwer Academic,2002 2. Kaushik Roy, Sharat Prasad, "Low power CMOS VLSI & EMBEDDED SYSTEM circuit design", John Wiley sons Inc.,2000. 3. J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI & EMBEDDED SYSTEM Circuits", Wiley,1999. 4. A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer,1995 4. Gary Yeap, "Practical low power digital VLSI & EMBEDDED SYSTEM design", Kluwer,1998.	

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VLSI & EMBEDDED SYSTEM

Class		**M.TECH.**	**L**	**T**	**P**	**C**
Semester/Year		**I/I**	**3**	**-**	**-**	**3**
Subject Name		**Communication Busses and Interfaces**				
Subject Code		**MECVES20S206**				
Paper	**English**					
	Hindi					
Max. Marks:		**100**				

Course Objective:

1. Serial Busses Physical interface. Limitations and applications of RS232. Data Streaming Serial Communication Protocol.

Course Outcomes:

At the end of the course, students will be able to:

CO1: Select a particular serial bus suitable for a particular application.
CO2: Develop APIs for configuration, reading and writing data onto serial bus.
CO3: Design and develop peripherals that can be interfaced to desired serial bus.
CO4: Understand Hardware protocols.
CO5: Understand Serial Front Panel Data Port (SFPDP) using fibre optic and copper cable.

Unit	Syllabus	Periods
UNIT-I	Serial Busses Physical interface, Data and Control signals, features.	**8**
UNIT-II	Limitations and applications of RS232, RS485, I^2C, SPI.	**9**
UNIT-III	CAN - Architecture, Data transmission, Layers, Frame formats,applications.	**11**

UNIT-IV	PCIe - Revisions, Configuration space, Hardware protocols, applications.	**13**
UNIT-V	USB - Transfer types, enumeration, Descriptor types and contents, Device driver. Data Streaming Serial Communication Protocol - Serial Front Panel Data Port (SFPDP) using fibre optic and copper cable	**14**
	Text Book(s) 1. Jan Axelson, "Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems ", Lakeview Research, 2nd Edition 2. Jan Axelson, "USB Complete", Penram Publications	
	Reference Book 1. Mike Jackson, Ravi Budruk, "PCI Express Technology", Mind share Press 2. Wilfried Voss, "A Comprehensible Guide to Controller Area Network", Copperhill Media Corporation, 2nd Edition,2005. 3. Serial Front Panel Draft Standard VITA 17.1 –200x	

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Class		M.TECH.	L	T	P	C
Semester/Year		II/I	3	-	-	3
Subject Name		Network Security and Cryptography				
Subject Code		MECVES20S207				
Paper	English					
	Hindi					
Max. Marks:		100				

Course Objective:

1. Explain Number Theory. Describe Private-Key (Symmetric) Cryptography. Public-Key (Asymmetric) Cryptography.

Course Outcomes:

ıe end of the course, students will be able to:

CO1: Identify and utilize different forms of cryptography techniques.
CO2: Incorporate authentication and security in the network applications.
CO3: Distinguish among different types of threats to the system and handle the same.
CO4: Understand Public-Key (Asymmetric) Cryptography.
CO5: Explain System Security.

Unit	Syllabus	Periods
UNIT-I	Need, security services, Attacks, OSI Security Architecture, one time passwords, Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptanalysis of Classical Encryption Techniques.	8

UNIT-II	Introduction, Fermat's and Euler's Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.	**9**
UNIT-III	Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES), Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Cryptanalysis.	**11**
UNIT-IV	RSA, Key Distribution and Management, Daffier-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4 MD5, Secure Hash algorithm, RIPEMD-160,HMAC.	**13**
UNIT-V	IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer and Transport Layer Security, Secure Electronic Transaction.	**14**
	Text Book(s): 1. Stallings, "Cryptography and Network Security, Principles and Practices", Pearson Education, 3rd Edition. 2. Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security, Private Communication in a Public World", Prentice Hall, 2ndEdition	
	Reference Book: 1. Christopher M. King, Ertem Osmanoglu, Curtis Dalton, "Security Architecture, Design Deployment and Operations", RSA Pres, 2. Stephen Northcutt, Leny Zeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, "Inside Network Perimeter Security", Pearson Education, 2ndEdition. 3. Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding Incident.	

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VLSI & EMBEDDED SYSTEM

Class		**M.TECH.**	**L**	**T**	**P**	**C**
Semester/Year		**II/I**	**3**	**-**	**-**	**3**
Subject Name		**Physical Design Automation**				
Subject Code		**MECVES20S208**				
Paper	**English**					
	Hindi					
Max. Marks:		**100**				

Course Objective:

1. Introduction to VLSI & EMBEDDED SYSTEM Physical Design Automation. Describe Standard cell. Explain Over the Cell Routing.

Course Outcomes:

At the end of the course, students will be able to:

CO1: Study automation process for VLSI & EMBEDDED SYSTEM System design.
CO2: Understand fundamentals for various physical design CAD tools.
CO3: Develop and enhance the existing algorithms and computational techniques for physical design process of VLSI & EMBEDDED SYSTEM systems.
CO4: Study Timing-driven placement.
CO5: Understand Over the Cell Routing.

Unit	Syllabus	Periods
UNIT-I	Introduction to VLSI & EMBEDDED SYSTEM Physical Design Automation.	**8**
UNIT-II	Standard cell, Performance issues in circuit layout, delay models Layout styles.	**9**

UNIT-III	Discrete methods in global placement.	**11**
UNIT-IV	Timing-driven placement. Global Routing Via Minimization.	**13**
UNIT-V	Over the Cell Routing - Single layer and two-layer routing, Clock and Power Routing. Compaction, algorithms, Physical Design Automation of FPGAs.	**14**
	Text Book(s): 1. William Stallings, "Cryptography and Network Security, Principles and Practices", Pearson Education, 3rd Edition. 2. Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security, Private Communication in a Public World", Prentice Hall, 2ndEdition	
	Reference Book: 1. Christopher M. King, ErtemOsmanoglu, Curtis Dalton, "Security Architecture, Design Deployment and Operations", RSAPres, 3. Stephen Northcutt, LenyZeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, "Inside Network Perimeter Security", Pearson Education, 2ndEdition 4. Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding Incident 5. Detection and Response", William Pollock Publisher, 2013.	

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VLSI & EMBEDDED SYSTEM

Class		**M.TECH.**	**L**	**T**	**P**	**C**
Semester/Year		**II/I**	**-**	**-**	**4**	**2**
Subject Name		**Mini Project**				
Subject Code		**MECVES20S209**				
Paper	**English**					
	Hindi					
Max. Marks:		**50**				

Course objective:

1. The students will be able to understand and apply the knowledge of management functions like planning, scheduling, executing and controlling to projects. The students will be able to implement the safety aspects during the execution project.

Course Outcomes:

At the end of the course, the student will be able to:

CO1: Identify structural engineering problems reviewing available literature.

CO2: Study different techniques used to analyze complex structural systems.

CO3: Work on the solutions given and present solution by using his/her technique applying engineering principles.

Unit	Syllabus	Periods
	Mini Project will have mid semester presentation and end semester presentation. Mid semester presentation will include identification of the problem based on the literature review on the topic referring to latest literature available. End semester presentation should be done along with the report on identification of topic for the work and the methodology adopted involving scientific research, collection and analysis of data, determining solutions highlighting individuals' contribution. Continuous assessment of Mini Project at Mid-Sem and End-Sem will be monitored by the departmental committee.	

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Estd. by Madhya Pradesh Niji Vishvavidyalaya (Sthapna Evam Sanchalana) Adhyadesh, 2020

SCHOOL OF ENGINEERING

SYLLABUS

VLSI & EMBEDDED SYSTEM

Class		M.TECH.	L	T	P	C
Semester/Year		II/I	2	-	-	-
Subject Name		Stress Management by Yoga				
Subject Code		MECVES20S210				
Paper	English					
	Hindi					
Max. Marks:		-				

Course Objective:

After completing this module, you should be able to:
1. To achieve overall health of body and mind. To overcome stress.

Course Outcomes:

After completion of course, students would be able to:

CO1: Develop healthy mind in a healthy body thus improving social health.

CO2: Improve efficiency.

Unit	Syllabus	Periods
UNIT-I	Definitions of Eight parts of yog. (Ashtanga)	**8**
UNIT-II	Yam and Niyam. Do`s and Don't sin life. i) Ahinsa, satya, astheya, bramh Acharya and aparigraha ii) Shaucha, santosh, tapa, swadhyay,ishwarpranidhan	**9**

UNIT-III	Asanand Pranayam i) Various yog poses and their benefits for mind &body **ii)**Regularization of breathing techniques and its effects-Types of pranayam	**11**
	Reference Books: 1. Yogic Asanasfor Group Tarining -Part-I": Janardan Swami Yogabhyasi Mandal, Nagpur. 2. Rajayoga or conquering the Internal Nature" by Swami Vivekananda, AdvaitaAshrama (Publication Department),Kolkata	

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Class		**M.TECH.**	**L**	**T**	**P**	**C**
Semester/Year		**II/I**	**-**	**-**	**4**	**2**
Subject Name		**Analog and Digital CMOS VLSI Design Lab**				
Subject Code		**MECVES20S211**				
Paper	**English**					
	Hindi					
Max. Marks:		**50**				

	List of Experiments: 1) Use VDD=1.8V for 0.18um CMOS process, VDD=1.3V for 0.13um CMOS Process and VDD=1V for 0.09um CMOS Process. a) Plot ID vs. VGS at different drain voltages for NMOS,PMOS. b) Plot ID vs. VGS at particular drain voltage (low) for NMOS, PMOS and determine Vt. c) Plot log ID vs. VGS at particular gate voltage (high) for NMOS, PMOS and determine IOFF and sub-threshold slope. d) Plot ID vs. VDS at different gate voltages for NMOS, PMOS and determine Channel length modulation factor. e) Extract Vth of NMOS/PMOS transistors (short channel and long channel). Use VDS = 30mV To extract Vth use the following procedure. i. Plot gmvs VGS using NGSPICE and obtain peak gmpoint. ii. Plot y=ID/(gm)1/2 as a function of VGS usingNgspice. iii. Use Ngspicetoplot tangent line passing through peak gm	

point in y (VGS) plane and determineVth.

f) Plot ID vs. VDS at different drain voltages for NMOS, PMOS, plot DC load line and calculate gm, gds, gm/gds, and unity gainfrequency.

Tabulate your result according to technologies and comment on it.

2) Use VDD=1.8V for 0.18um CMOS process, VDD=1.2V for 0.13um CMOS Process and VDD=1V for 0.09um CMOSProcess.

a) Perform thefollowing

i. Plot VTC curve for CMOS inverter and thereon plot dVoutvs. dVin and determine transition voltage and gain g. Calculate VIL, VIH, NMH, NML for theinverter.

ii. Plot VTC for CMOS inverter with varyingVDD.

iii. Plot VTC for CMOS inverter with varying deviceratio.

b) Perform transient analysis of CMOS inverter with no load and with load and determine tpHL, tpLH, 20%-to-80% trand 80%-to-20% tf. (use VPULSE = 2V, Cload =50fF)

c) Perform AC analysis of CMOS inverter with fanout 0 and fanout1. (Use Cin= 0.012pF, Cload = 4pF, Rload =k)

3) Use Ngspicetobuilda three stage and five stage ring oscillator circuit in 0.18um and 0.13um technology and compare its frequencies and timeperiod.

4) Perform thefollowing

a) Draw small signal voltage gain of the minimum-size inverter in 0.18um and 0.13um technology as a function of input DC voltage. Determine the small signal voltage gain at the switching point using Ngspice and compare the values for 0.18um and 0.13umprocess.

b) Consider a simple CS amplifier with active load, as explained in the lecture, with NMOS transistor MN as driver and PMOS transistor MP as load, in 0.18um technology. (W/L)MN=5, (W/L)MP=10 and L=0.5um for both transistors.

i. Establish a test bench, as explained in the lecture, to achieveVDSQ=VDD/2.

ii. Calculate input bias voltage if biascurrent=50uA.

iii. Use Ngspice and obtain the bias current. Compare its value with50uA.

iv. Determine small signal voltage gain, -3dB BW and GBW of the amplifier using small signal analysis in Ngspice (consider 30fF load capacitance).

v. Plot step response of the amplifier for input pulse amplitude of

0.1V. Derive time constant of the output and compare it with the time constant resulted from -3dBBW

vi. Use Ngspice to determine input voltage range of theamplifier

5) ThreeOPAMPINA.Vdd=1.8VVss=0V,CADtool:MentorGraphicsDA.

Note: Adjust accuracy options of the simulator (setup->options inGUI).Use proper values of resistors to get a three OPAMP INA with differential-mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the secondstage.

i. Draw the schematic of op-amp macromodel.
ii. Draw the schematic ofINA.
iii. Obtain parameters of the op-amp macro model suchthat
    a. low-frequency voltage gain =5x104,
    b. unity gain BW (fu) =500KHz,
    c. inputcapacitance=0.2pF,
    d. output resistance =,
    e. CMRR=120dB
iv. Draw schematic diagram of CMRR simulationsetup.
v. Simulate CMRR of INA using AC analysis (it's expected to be around 6dB below CMRR ofOPAMP).
vi. Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. Explain how CMRR of OPAMP changes with resistormismatches.
vii. Repeat (iii) to (vi) by considering CMRR of all OPAMPs to be90dB.

6) Technology: UMC 0.18um, VDD=1.8V. Use MAGIC orMicrowind.
    a) Draw layout of a minimum size inverter in UMC 0.18um technology using MAGIC Station layout editor. Use that inverter as a cell and lay out three cascaded minimum-sized inverters. Use M1 as interconnect line between inverters.
    b) Run DRC, LVS and RC extraction. Make sure there is no DRC error. Extract the netlist.
    c) Use extracted netlist and obtain tPHLtPLH for the middle inverter using Eldo.
    d) Use interconnect length obtained and connect the second and thirdinverter.

2. Extract the new netlist and obtain tPHL and tPLH of the middle inverter. Compare new values of delay times with corresponding values obtained in part ‘c’.

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Semester/Year		**II/I**	**-**	**-**	**4**	**2**
Subject Name		**VLSI Design Verification and Testing Lab**				
Subject Code		**MECVES20S212**				
Paper	**English**					
	Hindi					
Max. Marks:		**50**				

List of Experiments:

1. Sparse memory
2. Semaphore
3. Mailbox
4. Classes
5. Polymorphism
6. Coverage
7. Assertions